

## CLAIMS

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1. A processing system for accessing memory, comprising:  
an address bus for providing a current address and a previous address to  
memory;  
a data bus for receiving information from memory; and  
first means for generating a first sequence signal that when negated  
indicates that the current address may not be sequential to the  
previous address, a second sequence signal that when negated  
indicates that the current address is not sequential to the previous  
address, and a third sequence signal that when negated indicates that  
the current address, if it is an instruction address, is not sequential to  
the previous address that was an instruction address.
2. The processing unit of claim 1, wherein if the current address is not  
sequential to the previous address, the first sequence signal is negated prior to  
the second sequence signal being negated.
3. A processing system for accessing memory, comprising;  
an address bus for providing a current address and a previous address to  
memory;  
a data bus for receiving information from memory  
an execution unit which generates branch conditions and data addresses;  
a decode control unit which decodes instructions; and

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5 a fetch unit, coupled to the execution unit, the decode control unit, the address bus, and the data bus, for generating a first sequence signal that when negated indicates that the current address may not be sequential to the previous address, a second sequence signal that when negated indicates that the current address is not sequential to the previous address, and a third sequence signal that when negated indicates that the current address, if it is an instruction address, is not sequential to the previous address that was an instruction address.

10 4. The processing system of claim 3, wherein the decode control unit comprises an instruction register.

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15 5. The processing system of claim 3, wherein the fetch unit comprises: an address control unit, coupled to the decode control unit and the execution unit, for receiving a branch condition signal from the execution unit and a branch decode signal and a load/store signal from the decode unit and for providing the first, second, and third sequence signal.

20 6. The processing system of claim 5, wherein the execution unit comprises a condition generator that provides the branch condition signal.

25 7. The processing system of claim 6, wherein the execution unit comprises a data address generator which provides a data address signal to the fetch unit.

8. The processing system of claim 7, wherein if the current address is not sequential to the previous address, the first sequence signal is negated prior to the second sequence signal being negated.

5 9. The processing system of claim 3, wherein if the current address is not sequential to the previous address, the first sequence signal is negated prior to the second sequence signal being negated

10 10. A processing system for fetching instructions and data, comprising:  
an address bus for providing a current address for retrieving a first  
instruction, a previous address for retrieving a second instruction, and  
a data address for retrieving data, wherein the data address occurs  
before the current address and after the previous address;  
a data bus for retrieving the first and second instructions and the data; and  
15 a fetch unit, coupled to the address bus and the data bus, for generating a  
first sequence signal that when asserted for the current address  
indicates that the current address is sequential to the previous address  
and when negated indicates that the current address may not be  
sequential to the previous address.

20 11. The processing system of claim 10, wherein the fetch unit comprises:  
an address control unit for receiving a branch condition, a branch decode  
signal, and a load/store signal and for providing the first sequence  
signal.

25 12. The processing system of claim 11, further comprising:

an execution unit which provides the branch condition unit; and  
a decode control unit which provides the branch decode signal and the  
load/store signal.

5 13. A processing system comprising:  
an execution unit;  
a decode control unit;  
a fetch unit, coupled to the execution unit and the decode unit, for  
providing addresses on an address bus which may be sequential, and  
10 providing a first sequence signal which indicates if a current address  
may be sequential to a previous address and a second sequence signal  
which indicates if the current address is sequential to the previous  
address.

15 14. The processing system of claim 13, wherein if the second sequence signal  
indicates that the current address is not sequential to the previous address, the  
first sequence signal indicates that the current address may not be sequential to  
the previous address prior to the second sequence signal indicating that the  
current address is not sequential to the previous address.

20 15. The processing system of claim 14, wherein the addresses may be  
instruction addresses, and wherein the fetch unit further provides a third  
sequential signal which indicates if a current instruction address is sequential to  
a previous instruction address.

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16. The processing unit of claim 15, wherein the execution unit comprises a condition generator that provides a branch condition signal to the fetch unit.

Q1 5 17. The processing unit of claim 16, wherein the decode control unit provides a branch decode signal and a load/store signal to the fetch unit.

18. A processing unit comprising:

an execution unit;

a decode control unit;

10 a fetch unit, coupled to the execution unit and the decode unit, for providing instruction and data addresses on an address bus and providing a first sequence signal that indicates if a current instruction address is sequential to a previous instruction address even if a data address is provided between the current instruction address and the previous instruction address.

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19. The processing unit of claim 18, wherein the execution unit comprises a condition generator that provides a branch condition signal to the fetch unit.

20 20. The processing unit of claim 19, wherein the decode control unit provides a branch decode signal and a load/store signal to the fetch unit.

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